We Claim:

1. An improved test structure for determining a resistance of a conducting junction between an active region of a selection transistor and a storage capacitor in a matrix-type cell array, wherein:

the matrix cell array has active regions of selection transistors arranged in rows along a first direction and storage capacitors arranged in rows along a second direction perpendicular to the first direction; and

conducting junctions between the active regions of the selection transistors and the storage capacitors are formed at overlapping areas of the rows running perpendicular to one another in each case in a single edge region of the overlapping area in the first direction;

the improvement which comprises:

the active regions of the selection transistors and/or the storage capacitors are connected by connecting structures selected from the group consisting of tunnel structures and bridge structures in the second direction in the region adjoining the junction to be measured between the active region of the selection transistor and the storage capacitor,

for attaining a low-impedance connection to the junction to be measured.

2. The test structure according to claim 1, wherein, for determining a resistance of a series circuit comprising a plurality of the conducting junctions between active regions of selection transistors and storage capacitors in a row in the second direction, the corresponding active regions of the selection transistors and the corresponding storage capacitors are alternately connected via tunnel structures and bridge structures in the second direction.

3. The test structure according to claim 2, wherein the matrix-type cell array is a checkerboard array, the conducting junctions between the active regions of the selection transistors and the storage capacitors are formed at overlapping areas of the rows running perpendicular to one another in each case at every other overlapping area in a row in the first direction, the overlapping areas with the conducting junctions of rows lying next to one another in the first direction are offset with respect to one another, the current path for determining the resistance of the series circuit comprising a plurality of conducting junctions between active regions of selection transistors and the storage capacitors in a row in the second direction have a rectangular course with an alternating sequence of active regions of the

selection transistors connected via tunnel structures or bridge structures in the second direction and of storage capacitors connected via tunnel structures or bridge structures in the second direction.

4. The test structure according to claim 3, wherein, for determining the resistance of a series circuit comprising a plurality of conducting junctions between active regions of selection transistors and storage capacitors, a plurality of rows of series circuits comprising a plurality of conducting junctions between active regions of selection transistors and storage capacitors in the second direction are connected in a cell edge region via tunnel structures or bridge structures between the active regions of the selection transistors.

5. The test structure according to claim 1, wherein the matrix-type cell array is a checkerboard array, the conducting junctions between the active regions of the selection transistors and the associated storage capacitors are formed at overlapping areas of the rows running perpendicular to one another in each case at every other overlapping area in a row in the first direction, the overlapping areas with the conducting junctions of rows lying next to one another in the first direction are offset with respect to one another, the current path for determining the resistance of the conducting junction between the active region of the selection transistor

and the storage capacitor have an L-shaped course with active regions and/or storage capacitors connected via tunnel structures or bridge structures in the second direction.

6. The test structure according to claim 5, wherein a voltage path for determining the resistance of the conducting junction between the active region of the selection transistor and the storage capacitor has an L-shaped course with active regions and/or storage capacitors connected via tunnel structures or bridge structures in the second direction, a current path and the voltage path are disposed mirror-symmetrically with respect to the active region with the conducting junctions in the first direction.